CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An MIS capacitor comprising:

a lower electrode formed over a semiconductor substrate;

a dielectric layer comprising aluminum oxide formed over said lower electrode; and

a metal nitride upper electrode formed over said dielectric layer.

2. The MIS capacitor of claim 1, wherein said dielectric layer further comprises a material incorporated with said aluminum oxide.

3. The MIS capacitor of claim 2, wherein said material is selected from the group consisting of tantalum oxide, zirconium oxide, hafnium oxide, hafnium-aluminum-oxygen alloys and lanthanum-aluminum-oxygen alloys.

4. The MIS capacitor of claim 3, wherein said dielectric layer comprises aluminum oxide and tantalum oxide.

5. The MIS capacitor of claim 3, wherein said dielectric layer is formed of interleaved layers of aluminum oxide and tantalum oxide.

6. The MIS capacitor of claim 1, wherein said dielectric layer comprises an aluminum oxide /tantalum oxide /aluminum oxide composite stack.

7. The MIS capacitor of claim 1, wherein said dielectric layer consists essentially of an aluminum oxide dielectric layer.

8. The MIS capacitor of claim 1, wherein said dielectric layer is an ALD aluminum oxide layer.

9. The MIS capacitor of claim 8, wherein said dielectric layer is an annealed ALD aluminum oxide layer.

10. The MIS capacitor of claim 8, wherein said ALD aluminum oxide layer has a thickness of about 10 Angstroms to about 100 Angstroms.

11. The MIS capacitor of claim 1, wherein said upper electrode is a tungsten nitride layer.

12. The MIS capacitor of claim 11, wherein said upper electrode is an ALD tungsten nitride layer.

13. The MIS capacitor of claim 12, wherein said ALD tungsten nitride layer is a nitridized ALD tungsten nitride layer.

14. The MIS capacitor of claim 1, wherein said upper electrode is a titanium nitride layer.

15. The MIS capacitor of claim 14, wherein said upper electrode is an ALD titanium nitride layer.

16. The MIS capacitor of claim 15, wherein said ALD titanium nitride layer is a nitridized ALD titanium nitride layer.

17. The MIS capacitor of claim 1, wherein said upper electrode is a boron-doped titanium nitride layer.

18. The MIS capacitor of claim 17, wherein said boron-doped titanium nitride layer is a nitridized boron-doped titanium nitride layer.

19. The MIS capacitor of claim 18, wherein said boron-doped titanium nitride layer has a boron concentration of about 0.01% to about 30%.

20. The MIS capacitor of claim 1, wherein said lower electrode is formed of a material selected from the group consisting of hemispherical grained polysilicon, silica, germanium and silicon.

21. The MIS capacitor of claim 20, wherein said lower electrode is formed of hemispherical grained polysilicon.

22. The MIS capacitor of claim 21, wherein said lower electrode is formed of etched hemispherical grained polysilicon with activated hemispherical grained polysilicon grains.

23. The MIS capacitor of claim 22, wherein said etched hemispherical grained polysilicon is a nitridized etched hemispherical grained polysilicon.

24. The MIS capacitor of claim 22, wherein said etched hemispherical grained polysilicon is an annealed hemispherical grained polysilicon.

25. The MIS capacitor of claim 1 further comprising a silicon-doped layer at the interface between said lower electrode and said dielectric layer comprising aluminum oxide.

26. The MIS capacitor of claim 25, wherein said silicon-doped layer has a thickness of about 5 Angstroms to about 50 Angstroms.

27. The MIS capacitor of claim 25, wherein said silicon-doped layer is an aluminum-oxygen-silicon layer.

28. The MIS capacitor of claim 1 further comprising a metal-doped layer at the interface between said dielectric layer comprising aluminum oxide and said metal nitride upper electrode.

29. The MIS capacitor of claim 28, wherein said metal-doped layer has a thickness of about 5 Angstroms to about 100 Angstroms.

30. The MIS capacitor of claim 28, wherein said metal-doped layer is an aluminum-titanium-oxygen-nitrogen layer.

31. The MIS capacitor of claim 28, wherein said metal-doped layer comprises a metal similar to the metal of said metal nitride upper electrode.

32. A memory device comprising:

a substrate;

a memory cell formed over said substrate, said memory cell comprising a transistor including a gate fabricated on said substrate, and source and drain regions in said substrate disposed adjacent to said gate; and

a charge storage capacitor electrically connected to one of said source and drain regions, said capacitor comprising a semiconductive layer, an aluminum oxide dielectric layer formed over said semiconductive layer, and a metal nitride layer formed over said aluminum oxide dielectric layer.

33. The memory device of claim 32, wherein said aluminum oxide dielectric layer further comprises a material incorporated with said aluminum oxide.

34. The memory device of claim 33, wherein said material is selected from the group consisting of tantalum oxide, zirconium oxide, hafnium oxide, hafnium-aluminum-oxygen alloys and lanthanum-aluminum-oxygen alloys.

35. The memory device of claim 33, wherein said aluminum oxide dielectric layer further comprises tantalum oxide.

36. The memory device of claim 33, wherein said aluminum oxide dielectric layer is formed of interleaved layers of aluminum oxide and tantalum oxide.

37. The memory device of claim 33, wherein said aluminum oxide dielectric layer is an ALD aluminum oxide layer.

38. The memory device of claim 37, wherein said aluminum oxide dielectric layer is an annealed ALD aluminum oxide layer.

39. The memory device of claim 37, wherein said ALD aluminum oxide layer has a thickness of about 10 Angstroms to about 100 Angstroms.

40. The memory device of claim 32, wherein said metal nitride layer is a tungsten nitride layer.

41. The memory device of claim 40, wherein said metal nitride layer is an ALD tungsten nitride layer.

42. The memory device of claim 41, wherein said ALD tungsten nitride layer is a nitridized ALD tungsten nitride layer.

43. The memory device of claim 32, wherein said metal nitride layer is a titanium nitride layer.

44. The memory device of claim 43, wherein said metal nitride layer is an ALD titanium nitride layer.

45. The memory device of claim 44, wherein said ALD titanium nitride layer is a nitridized ALD titanium nitride layer.

46. The memory device of claim 32, wherein said metal nitride layer is a boron-doped titanium nitride layer.

47. The memory device of claim 46, wherein said boron-doped titanium nitride layer is a nitridized boron-doped titanium nitride layer.

48. The memory device of claim 47, wherein said boron-doped titanium nitride layer has a boron concentration of about 0.01% to about 30%.

49. The memory device of claim 32, wherein said semiconductive layer is formed of a material selected from the group consisting of hemispherical grained polysilicon, silica, germanium and silicon.

50. The memory device of claim 49, wherein said semiconductive layer is formed of hemispherical grained polysilicon.

51. The memory device of claim 50, wherein said semiconductive layer is formed of etched hemispherical grained polysilicon with activated hemispherical grained polysilicon grains.

52. The memory device of claim 51, wherein said etched hemispherical grained polysilicon is a nitridized etched hemispherical grained polysilicon.

53. The memory device of claim 51, wherein said etched hemispherical grained polysilicon is an annealed hemispherical grained polysilicon.

54. The memory device of claim 32, wherein said memory cell is a DRAM memory cell.

55. The memory device of claim 32, wherein said memory cell is a SRAM memory cell.

56. A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said integrated circuit and processor containing a capacitor, said capacitor comprising a hemispherical grained polysilicon lower capacitor electrode; an aluminum oxide dielectric layer formed over said lower capacitor electrode; and a metal nitride upper capacitor electrode formed over said aluminum oxide dielectric layer.

57. The processor-based system of claim 56, wherein said hemispherical grained polysilicon lower electrode is a nitridized hemispherical grained polysilicon lower electrode.

58. The processor-based system of claim 56, wherein said aluminum oxide dielectric layer is an ALD aluminum oxide dielectric layer.

59. The processor-based system of claim 58, wherein said aluminum oxide dielectric layer is a nitridized ALD aluminum oxide dielectric layer.

60. The processor-based system of claim 56, wherein said aluminum oxide dielectric layer further comprises a material incorporated with said aluminum oxide.

61. The processor-based system of claim 60, wherein said material is selected from the group consisting of tantalum oxide, zirconium oxide, hafnium oxide, hafnium-aluminum-oxygen alloys and lanthanum-aluminum-oxygen alloys.

62. The processor-based system of claim 56, wherein said integrated circuit is a memory device.

63. The processor-based system of claim 62, wherein said memory device is a DRAM memory device.

64. The processor-based system of claim 62, wherein said memory device is a SRAM memory device.

65. A method of forming an MIS capacitor on a semiconductor substrate, comprising the acts of:

forming a semiconductive layer over a substrate;

forming a dielectric layer comprising aluminum oxide over said semiconductive layer by atomic layer deposition; and

forming a metal nitride layer over said dielectric layer.

66. The method of claim 65, wherein said semiconductive layer is formed of hemispherical grained polysilicon.

67. The method of claim 66 further comprising the act of opening the grains which form said layer of hemispherical grained polysilicon to activate said grains.

68. The method of claim 67, wherein said act of opening said grains further comprising etching said layer of hemispherical grained polysilicon to form an etched layer of hemispherical grained polysilicon.

69. The method of claim 69, wherein said act of etching said layer of hemispherical grained polysilicon further comprises contacting said layer of hemispherical grained polysilicon with a solution of HF.

70. The method of claim 69 further comprising the act of subjecting said layer of hemispherical grained polysilicon to an RTN process.

71. The method of claim 69 further comprising the act of subjecting said layer of hemispherical grained polysilicon to an anneal process.

72. The method of claim 69 further comprising the act of subjecting said layer of hemispherical grained polysilicon to a PH_3 anneal.

73. The method of claim 65, wherein said metal nitride layer is a titanium nitride layer formed by CVD.

74. The method of claim 65, wherein said metal nitride layer is a titanium nitride layer formed by ALD.

75. The method of claim 74, wherein said titanium nitride layer is formed by ALD using a nitrogen source and a titanium source precursor.

76. The method of claim 65, wherein said metal nitride layer is a boron-doped titanium nitride layer formed by CVD.

77. The method of claim 77, wherein said act of providing said boron-doped titanium nitride layer further comprises the act of incorporating boron into a titanium nitride layer.

78. The method of claim 78, wherein said act of incorporating boron into a titanium nitride layer further comprises the act of exposing said titanium nitride layer to B_2H_6.

79. The method of claim 79, wherein said act of incorporating boron into a titanium nitride layer further comprises the act of exposing said titanium nitride layer to B_2H_6 at a temperature of about 200°C to about 600°C.

80. The method of claim 65, wherein said metal nitride layer is a tungsten nitride layer formed by CVD.

81. The method of claim 65, wherein said metal nitride layer is a tungsten nitride layer formed by ALD.

82. The method of claim 65, wherein said metal nitride layer is a boron-doped tungsten nitride layer formed by CVD.

83. The method of claim 82, wherein said act of providing said boron-doped tungsten nitride layer further comprises the act of incorporating boron into a tungsten nitride layer.

84. The method of claim 65, wherein said aluminum oxide dielectric layer is formed by ALD using an ozone source and an aluminum source precursor.

85. The method of claim 86, wherein said aluminum source precursor is trimethyl-aluminum.

86. The method of claim 65, wherein said aluminum oxide dielectric layer is formed to a thickness of about 10 Angstroms to about 500 Angstroms.

87. The method of claim 86, wherein said aluminum oxide dielectric layer is formed to a thickness of about 25 Angstroms to about 100 Angstroms.

88. The method of claim 65, wherein said aluminum oxide dielectric layer further comprises a material selected from the group consisting of tantalum oxide, zirconium oxide, hafnium oxide, hafnium-aluminum-oxygen alloys and lanthanum-aluminum-oxygen alloys.

89. The method of claim 88, wherein said aluminum oxide dielectric layer is formed as a composite stack of at least one aluminum oxide layer and at least one tantalum oxide layer.

90. The method of claim 89, wherein said aluminum oxide dielectric layer is formed of interleaved layers of aluminum oxide and tantalum oxide.

91. The method of claim 90, wherein said aluminum oxide dielectric layer is an aluminum oxide /tantalum oxide /aluminum oxide stack.

92. A method of forming an aluminum oxide MIS capacitor on a semiconductor substrate, comprising the acts of:

forming a lower capacitor electrode of hemispherical grained polysilicon over said semiconductor substrate;

forming a dielectric composite stack comprising aluminum oxide over said lower capacitor electrode; and

forming an upper capacitor electrode of tungsten nitride over said dielectric composite stack.

93. The method of claim 92, wherein said dielectric composite stack is formed by ALD.

94. The method of claim 93, wherein said dielectric composite stack is formed of interleaved layers of aluminum oxide and another metal oxide material.

95. The method of claim 94, wherein said metal oxide material is selected from the group consisting of tantalum oxide, zirconium oxide, hafnium oxide, hafnium-aluminum-oxygen alloys and lanthanum-aluminum-oxygen alloys.

96. The method of claim 92 further comprising the act of subjecting said dielectric composite stack to a nitridizing treatment.

97. The method of claim 96 further comprising the act of subjecting said dielectric composite stack to a PH_3 anneal treatment.

98. The method of claim 92, wherein said tungsten nitride layer is formed by ALD using a tungsten source and a nitrogen source precursor.

99. The method of claim 92 further comprising the act of etching said hemispherical grained polysilicon to form an etched hemispherical grained polysilicon.

100. The method of claim 99, wherein said act of etching said hemispherical grained polysilicon further comprises contacting said hemispherical grained polysilicon with a solution of HF.

101. The method of claim 100 further comprising the act of subjecting said hemispherical grained polysilicon to a PH_3 anneal.

102. The method of claim 101 further comprising the act of subjecting said hemispherical grained polysilicon to an RTN treatment.

103. The method of claim 102 further comprising the act of subjecting said hemispherical grained polysilicon to a HF solution after said PH_3 anneal and before said RTN treatment.